**Ahsanullah University of Science and Technology A**

**CSE 3109 Digital System Design Quiz 1 22-05-17 Marks 20**

1. Design a combinational circuit using a PLA. The circuit accepts a 2-bit number and generates an output binary number equal to the cube of the input number. Derive the PLA program table for this circuit. **10**
2. Deign an arithmetic logic unit with three selection variables S2, S1 and S0, that generates the following arithmetic and logic operations. When S2 =0 the arithmetic operations are done and when S2 =1 the logical operations are done. **10**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| S1 | S0 | Cin = 0 | Cin = 1 | Cin = × (don’t care) |
| 0 | 0 | F = A | F = A + 1 | F = A+B (OR) |
| 0 | 1 | F = A – B – 1 | F = A – B | F = A⊕B (XOR) |
| 1 | 0 | F = B – A – 1 | F = B – A | F = AB (AND) |
| 1 | 1 | F = A + B | F = A + B +1 | F = A B (NAND) |

**Ahsanullah University of Science and Technology B**

**CSE 3109 Digital System Design Quiz 1 22 - 05 - 17 Marks 20**

1. Design a combinational circuit using a PLA. The circuit accepts a 2-bit number and generates an output binary number equal to the cube of the input number. Derive the PLA program table for this circuit. **10**
2. Deign an arithmetic logic unit with three selection variables S2, S1 and S0, that generates the following arithmetic and logic operations. When S2 =0 the arithmetic operations are done and when S2 =1 the logical operations are done. **10**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| S1 | S0 | Cin = 0 | Cin = 1 | Cin = × (don’t care) |
| 0 | 0 | F = A + 1 | F = A | F = AB (AND) |
| 0 | 1 | F = A – B | F = A – B – 1 | F = A⊕B (XOR) |
| 1 | 0 | F = B – A | F = B – A – 1 | F = A+B (OR) |
| 1 | 1 | F = A + B + 1 | F = A + B | F = A B (NAND) |

**Ahsanullah University of Science and Technology A**

**CSE 3109 Digital System Design Quiz 1 22-05-17 Marks 20**

1. Design a combinational circuit using a PLA. The circuit accepts a 4-bit number and generates an output binary number equal to the half of the input number. You have to consider both input and output as integer numbers. Derive the PLA program table for this circuit. **10**
2. Deign an arithmetic logic unit with three selection variables S2, S1 and S0, that generates the following arithmetic and logic operations. When S2 =0 the arithmetic operations are done and when S2 =1 the logical operations are done. **10**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| S1 | S0 | Cin = 0 | Cin = 1 | Cin = × (don’t care) |
| 0 | 0 | F = A | F = A + 1 | F = A+B (OR) |
| 0 | 1 | F = A – B – 1 | F = A – B | F = A⊕B (XOR) |
| 1 | 0 | F = B – A – 1 | F = B – A | F = AB (AND) |
| 1 | 1 | F = A + B | F = A + B +1 | F = A B (NAND) |

**Ahsanullah University of Science and Technology B**

**CSE 3109 Digital System Design Quiz 1 22 - 05 - 17 Marks 20**

1. Design a combinational circuit using a PLA. The circuit accepts a 4-bit number and generates an output binary number equal to the half of the input number. You have to consider both input and output as integer numbers. Derive the PLA program table for this circuit. **10**
2. Deign an arithmetic logic unit with three selection variables S2, S1 and S0, that generates the following arithmetic and logic operations. When S2 =0 the arithmetic operations are done and when S2 =1 the logical operations are done. **10**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| S1 | S0 | Cin = 0 | Cin = 1 | Cin = × (don’t care) |
| 0 | 0 | F = A + 1 | F = A | F = AB (AND) |
| 0 | 1 | F = A – B | F = A – B – 1 | F = A⊕B (XOR) |
| 1 | 0 | F = B – A | F = B – A – 1 | F = A+B (OR) |
| 1 | 1 | F = A + B + 1 | F = A + B | F = A B (NAND) |